



# NJG1129MD7

## ■ ABSOLUTE MAXIMUM RATINGS

$T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_i=50\ \text{ohm}$

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
Drain voltage	$V_{DD}$		5.0	V
Inverter voltage	$V_{INV}$		5.0	V
Control voltage	$V_{CTL}$		5.0	V
Input power	$P_{in}$	$V_{DD}=V_{INV}=2.8\text{V}$	+15	dBm
Power dissipation	$P_D$	4-layer FR4 PCB with through-hole (74.2x74.2mm), $T_j=150^{\circ}\text{C}$	1300	mW
Operating temperature	$T_{opr}$		-40~+85	$^{\circ}\text{C}$
Storage temperature	$T_{stg}$		-55~+150	$^{\circ}\text{C}$

## ■ ELECTRICAL CHARACTERISTICS1 (DC CHARACTERISTICS)

General conditions:  $V_{DD}=V_{INV}=2.8\text{V}$ ,  $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_i=50\ \text{ohm}$ , with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	$V_{DD}$		2.3	2.8	3.6	V
Inverter voltage	$V_{INV}$		2.3	2.8	3.6	V
Control voltage (High)	$V_{CTL(H)}$		1.5	1.85	3.6	V
Control voltage (Low)	$V_{CTL(L)}$		0	0	0.3	V
Operating current1	$I_{DD1}$	RF OFF, $V_{CTL}=1.85\text{V}$	-	5.0	8.0	mA
Operating current2	$I_{DD2}$	RF OFF, $V_{CTL}=0\text{V}$	-	1	5	$\mu\text{A}$
Inverter current1	$I_{INV1}$	RF OFF, $V_{CTL}=1.85\text{V}$	-	90	180	$\mu\text{A}$
Inverter current2	$I_{INV2}$	RF OFF, $V_{CTL}=0\text{V}$	-	15	40	$\mu\text{A}$
Control current	$I_{CTL}$	RF OFF, $V_{CTL}=1.85\text{V}$	-	5	10	$\mu\text{A}$

## ■ ELECTRICAL CHARACTERISTICS2 (High Gain mode)

General conditions:  $V_{DD}=V_{INV}=2.8V$ ,  $V_{CTL}=1.85V$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\text{ ohm}$ , with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating frequency	$f_{RF}$		470	620	770	MHz
Small signal gain1	Gain1		11.0	15.0	19.0	dB
Noise figure	NF	Exclude PCB & connector losses*1	-	1.4	1.9	dB
Input power at 1dB gain compression point1	$P_{-1dB(IN)1}$		-14.0	-6.0	-	dBm
Input 3rd order intercept point1	IIP3_1	$f1=f_{RF}$ , $f2=f_{RF}+100kHz$ , $P_{IN}=-25dBm$	-6.0	+1.0	-	dBm
RF IN VSWR1	VSWRi1		-	1.5	4.5	-
RF OUT VSWR1	VSWRo1		-	1.5	2.8	-

## ■ ELECTRICAL CHARACTERISTICS3 (Low Gain mode)

General conditions:  $V_{DD}=V_{INV}=2.8V$ ,  $V_{CTL}=0V$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\text{ ohm}$ , with application circuit.

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating frequency	$f_{RF}$		470	620	770	MHz
Small signal gain2	Gain2	Exclude PCB & connector losses*2	-6.0	-4.0	-	dB
Input power at 1dB gain compression point2	$P_{-1dB(IN)2}$		+5.0	+12.0	-	dBm
Input 3rd order intercept point2	IIP3_2	$f1=f_{RF}$ , $f2=f_{RF}+100kHz$ , $P_{IN}=-12dBm$	+14.0	+20.0	-	dBm
RF IN VSWR2	VSWRi2		-	1.5	3.0	-
RF OUT VSWR2	VSWRo2		-	1.5	2.8	-

\*1 Input PCB and connector losses: 0.036dB(at 470MHz), 0.053dB(at 770MHz)

\*2 Input & output PCB and connector losses: 0.072dB(at 470MHz), 0.105dB(at 770MHz)

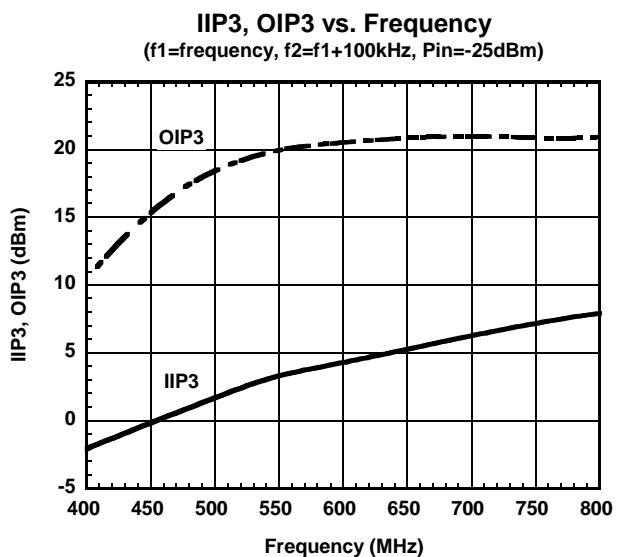
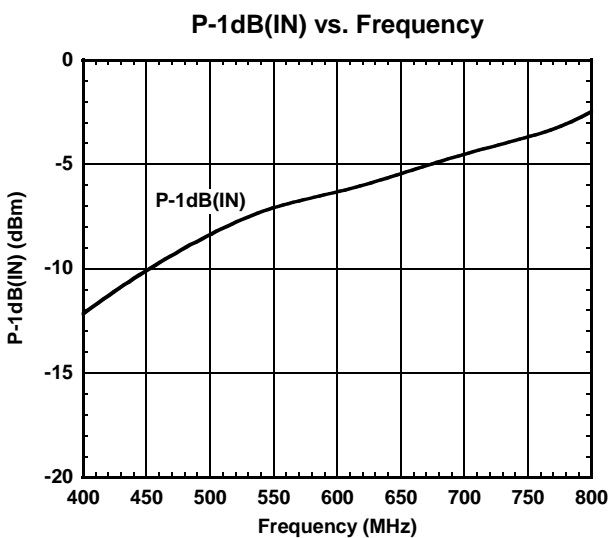
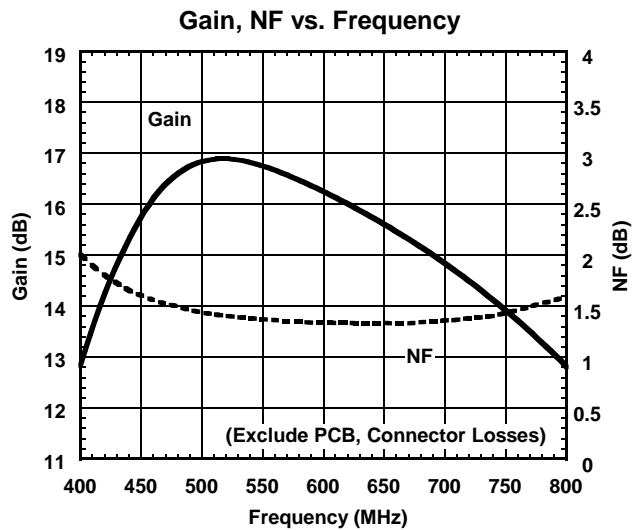
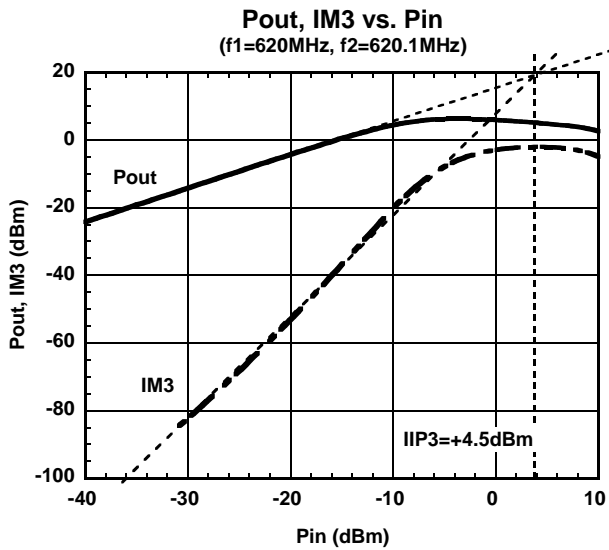
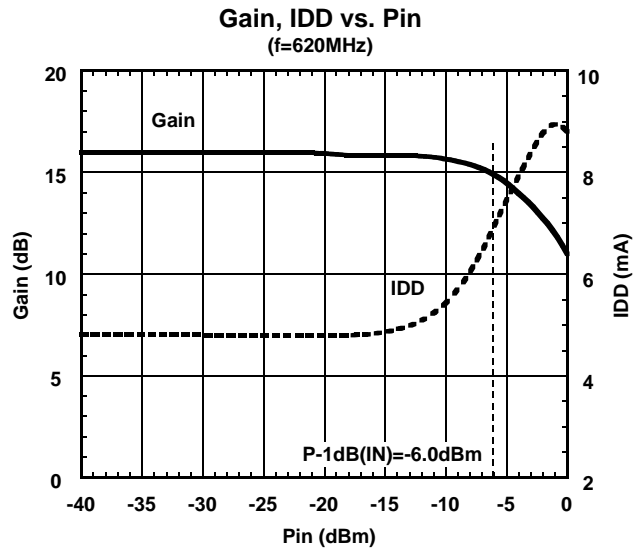
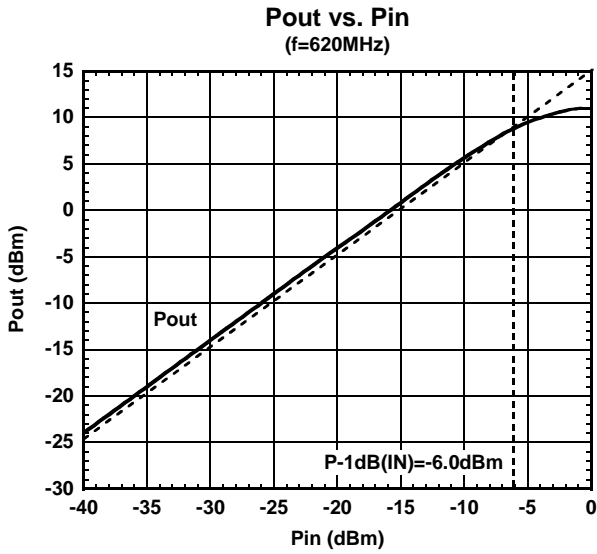
# NJG1129MD7

## ■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1, 2, 4, 5, 6, 8, 9, 10, 11, 13	GND	Ground terminal. These terminals should be connected to the ground plane as close as possible for excellent RF performance.
3	VINV	Inverter voltage supply terminal.
7	RFOUT	RF Output terminal. RF signal comes out from this terminal, and goes through an external matching circuit connected to this. Inductor L4 as shown in the application circuit is a part of an external matching circuit, and also provide DC power to LNA.
12	RFIN	RF input terminal. The RF signal is input through external matching circuit connected to this terminal. Since this IC is integrated an input DC blocking capacitor.
14	VCTL	Control voltage supply terminal.

## ■ ELECTRICAL CHARACTERISTICS (High Gain mode)

Conditions:  $T_a=+25^{\circ}\text{C}$ ,  $V_{DD}=V_{INV}=2.8\text{V}$ ,  $V_{CTL}=1.85\text{V}$ ,  $Z_s=Z_l=50\text{ ohm}$ , with application circuit

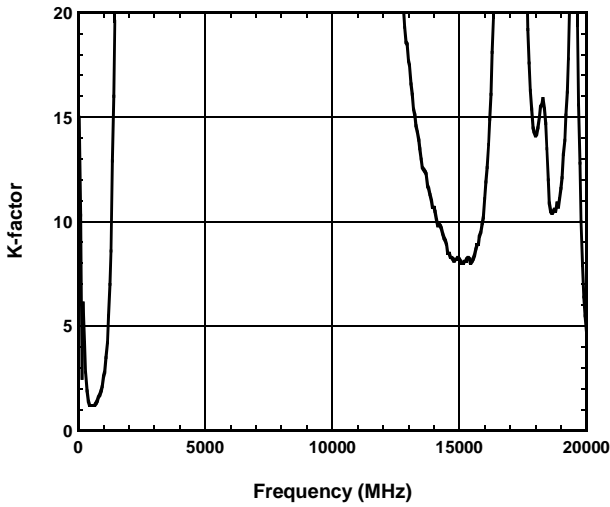


# NJG1129MD7

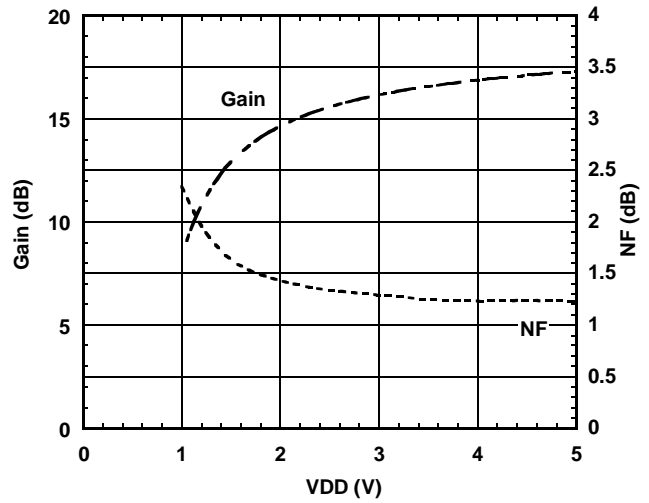
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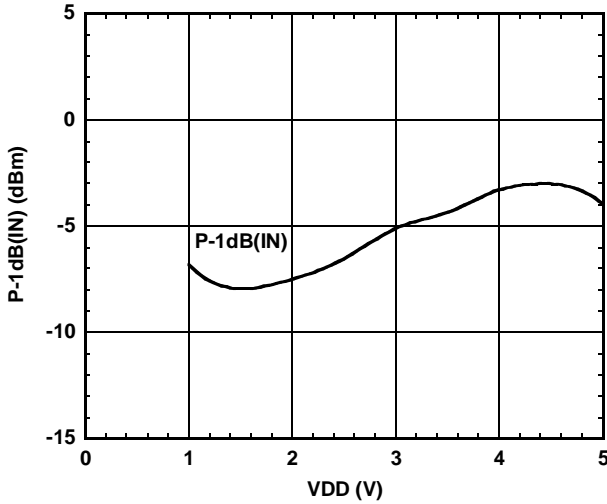
**K-factor vs. Frequency**



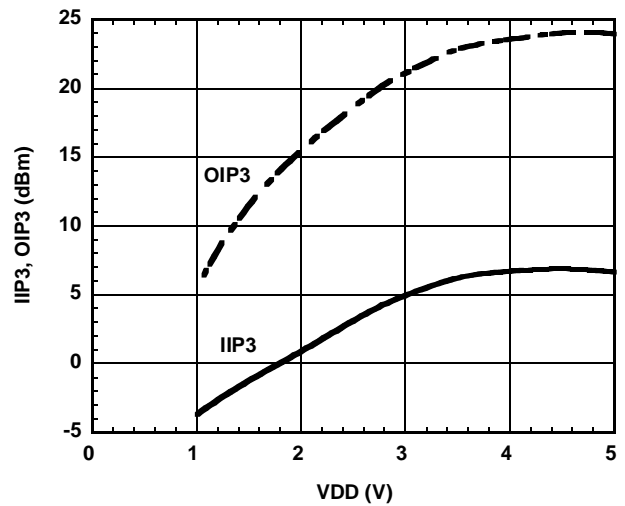
**Gain, NF vs. VDD=VINV (f=620MHz)**



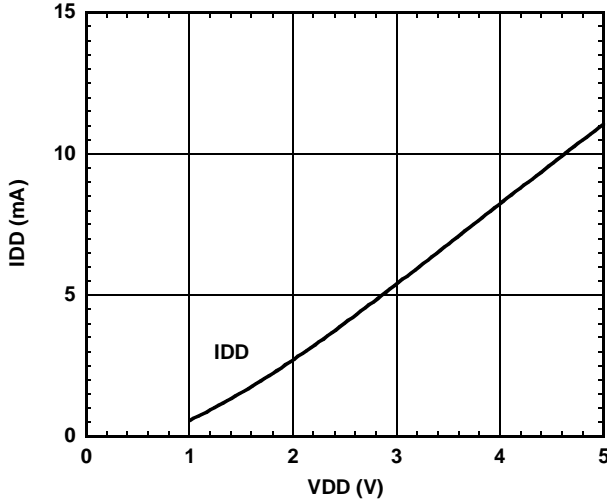
**P-1dB(IN) vs. VDD=VINV (f=620MHz)**



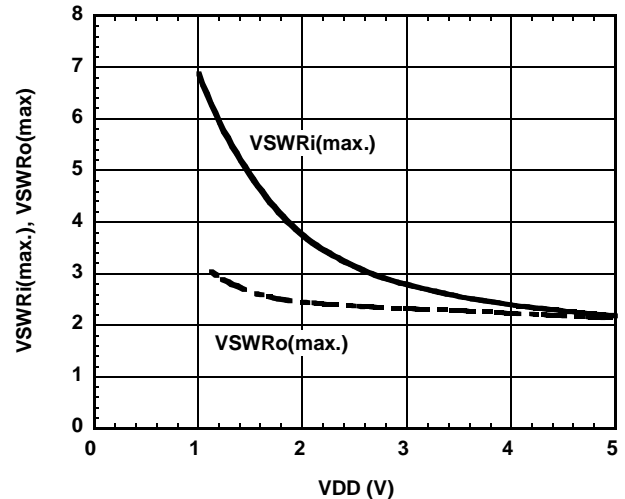
**IIP3, OIP3 vs. VDD=VINV (f1=620MHz, f2=620.1MHz, Pin=-25dBm)**



**IDD vs. VDD=VINV**

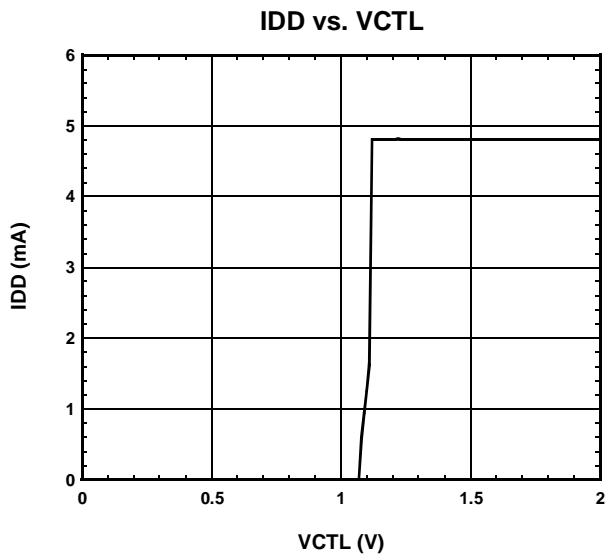


**VSWR vs. VDD=VINV**



## ■ ELECTRICAL CHARACTERISTICS (High Gain mode)

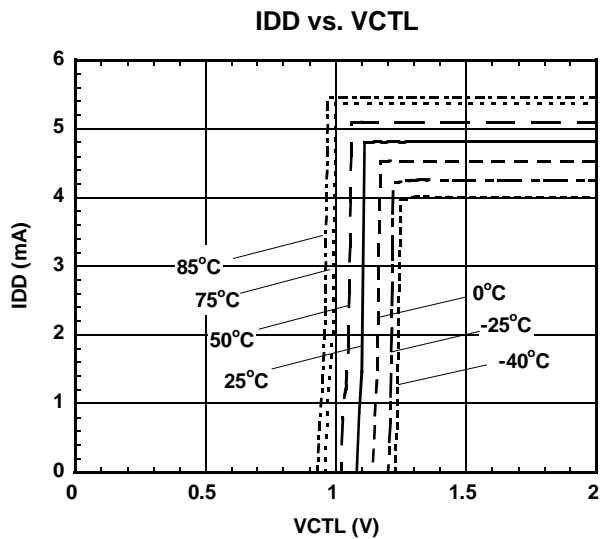
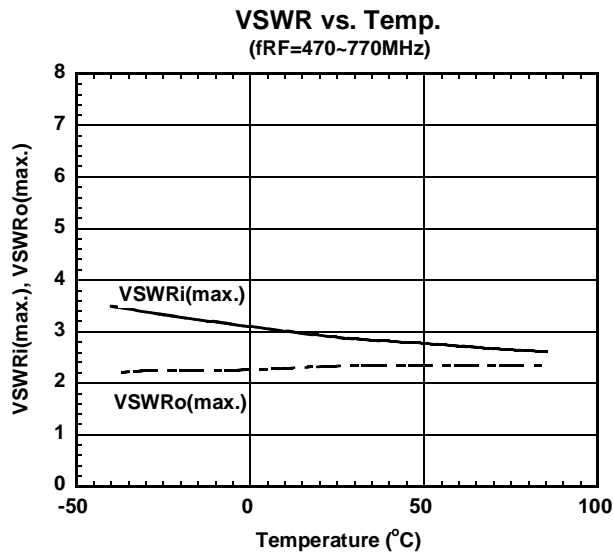
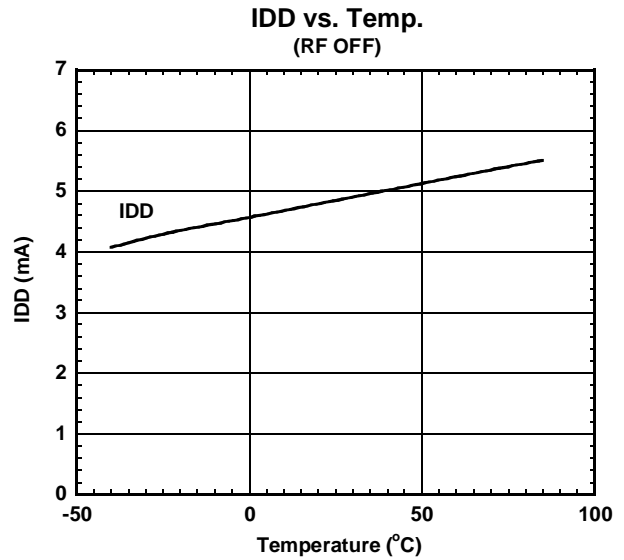
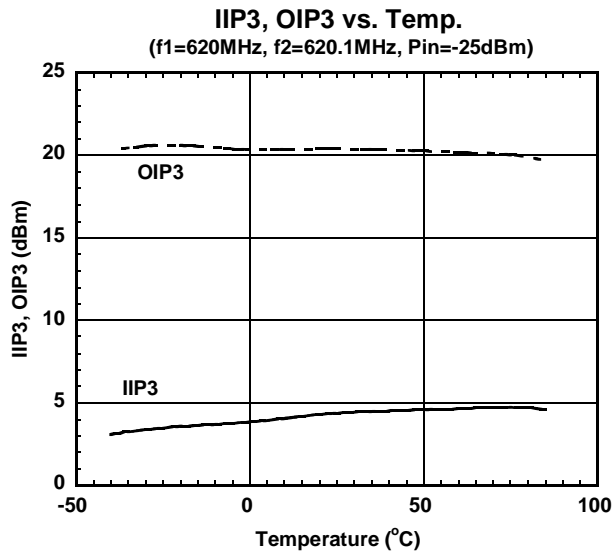
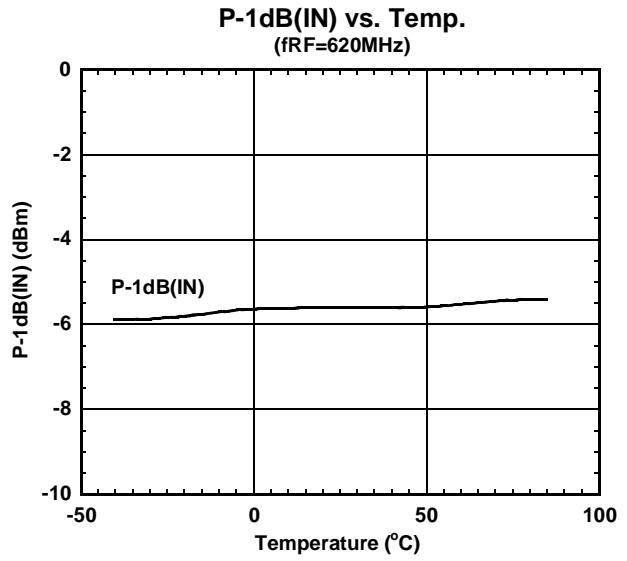
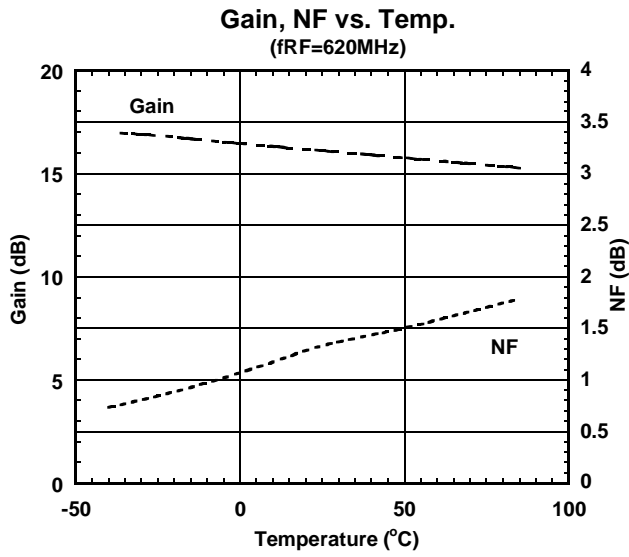
Conditions:  $T_a=+25^{\circ}\text{C}$ ,  $V_{DD}=2.8\text{V}$ ,  $Z_s=Z_l=50\text{ ohm}$ , with application circuit



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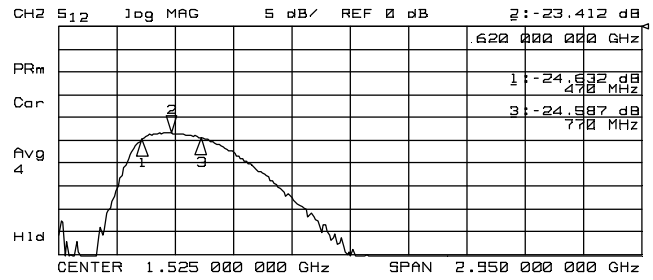
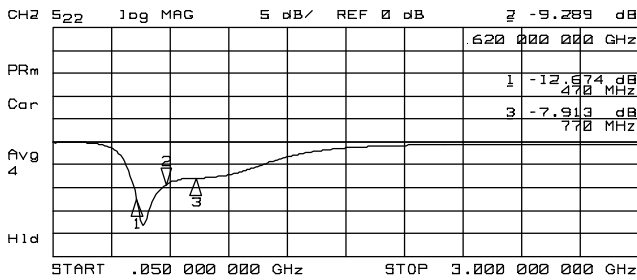
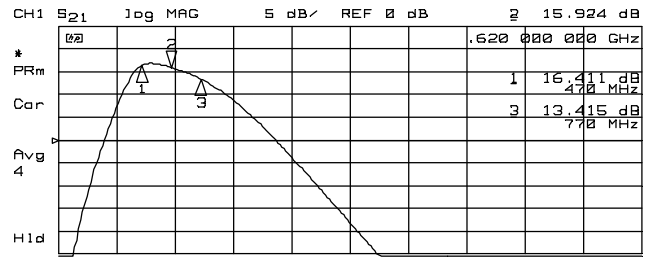
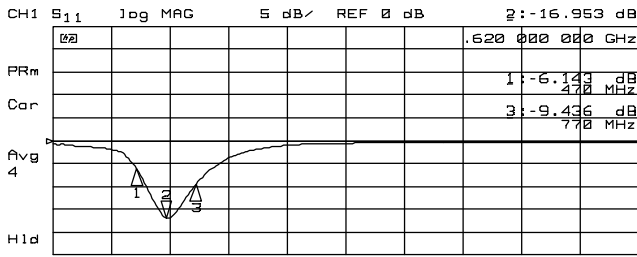
Conditions:  $V_{DD} = V_{INV} = 2.8V$ ,  $V_{CTL} = 1.85V$ ,  $Z_s = Z_l = 50\ \Omega$ , with application circuit





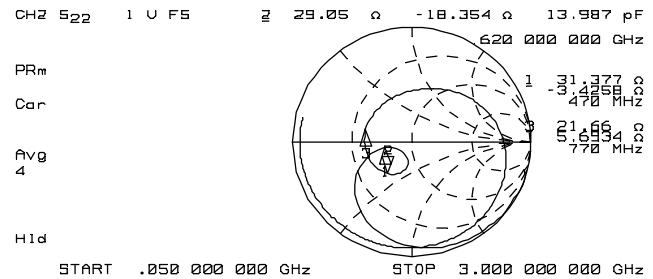
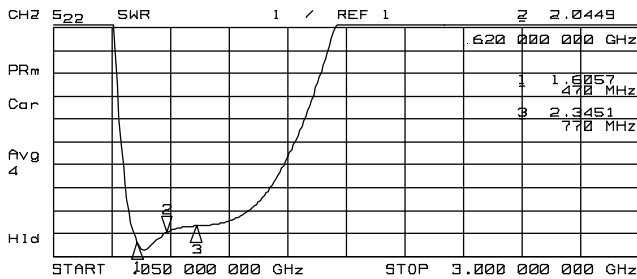
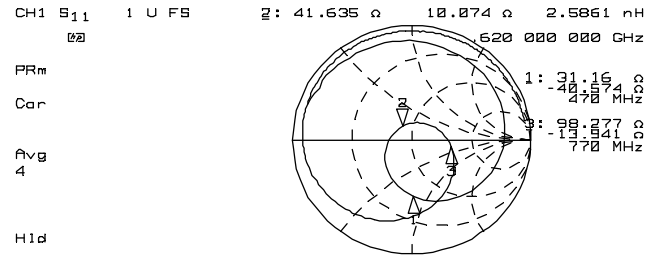
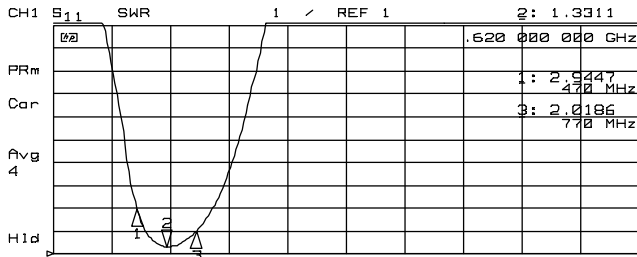
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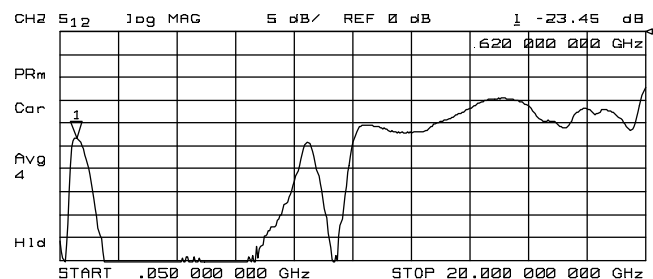
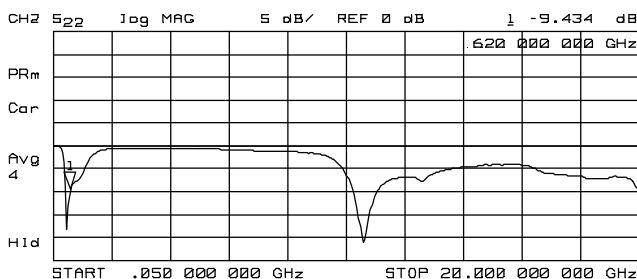
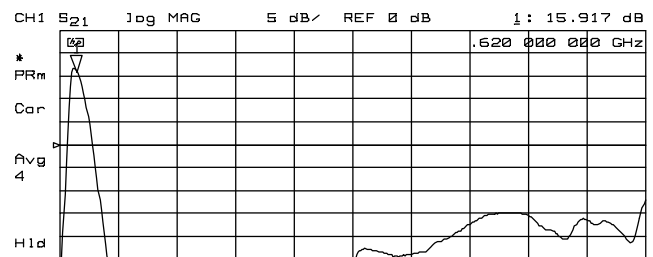
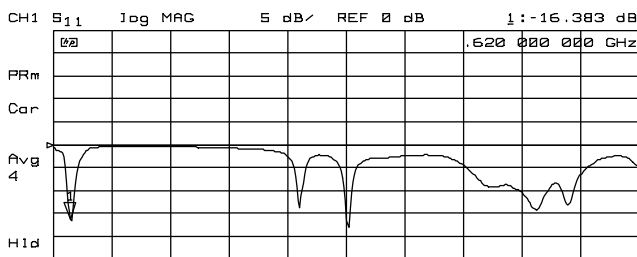
**S<sub>11</sub>, S<sub>22</sub>**

**S<sub>21</sub>, S<sub>12</sub>**



**VSWR**

**Z<sub>in</sub>, Z<sub>out</sub>**



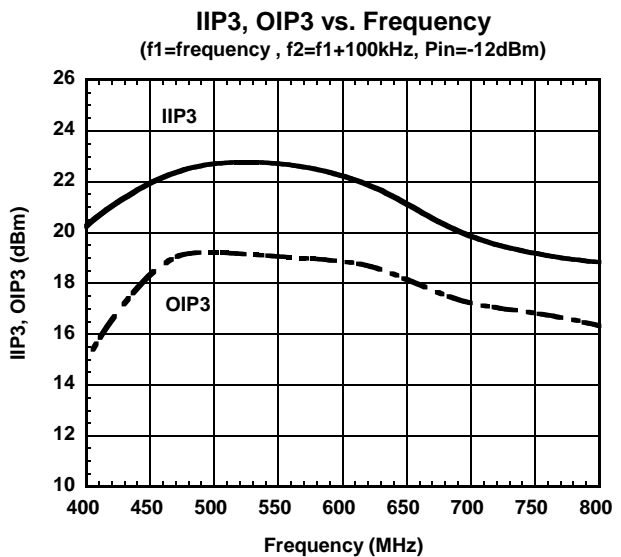
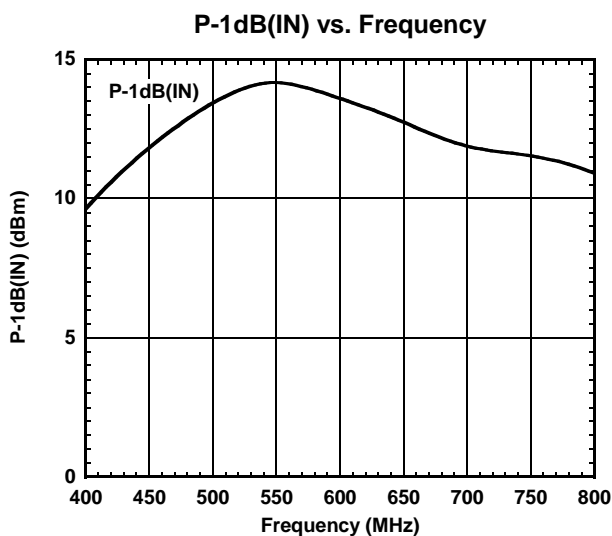
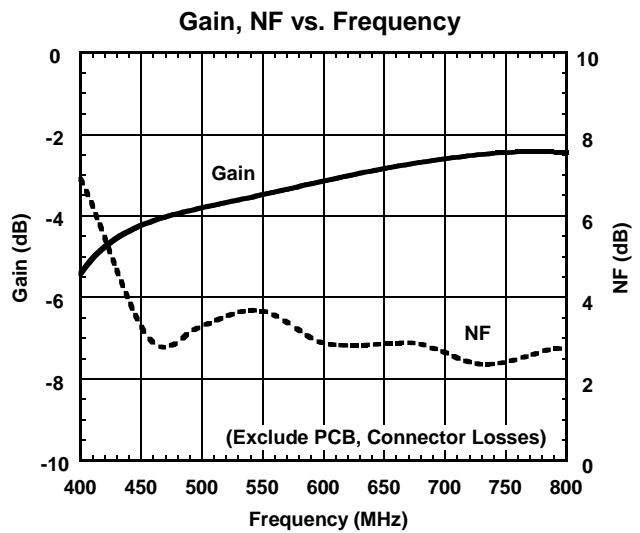
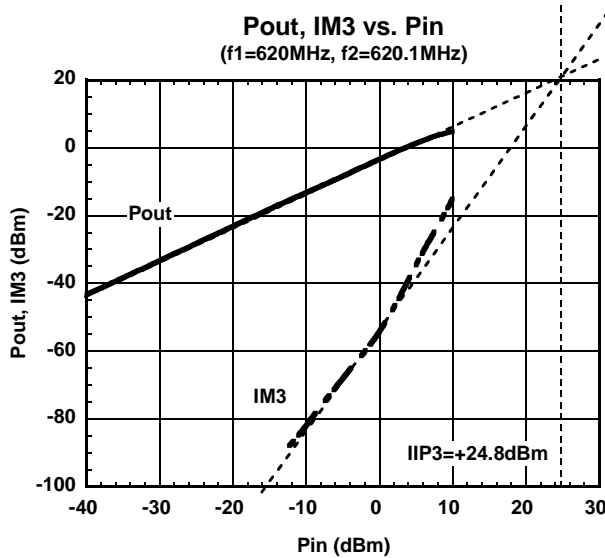
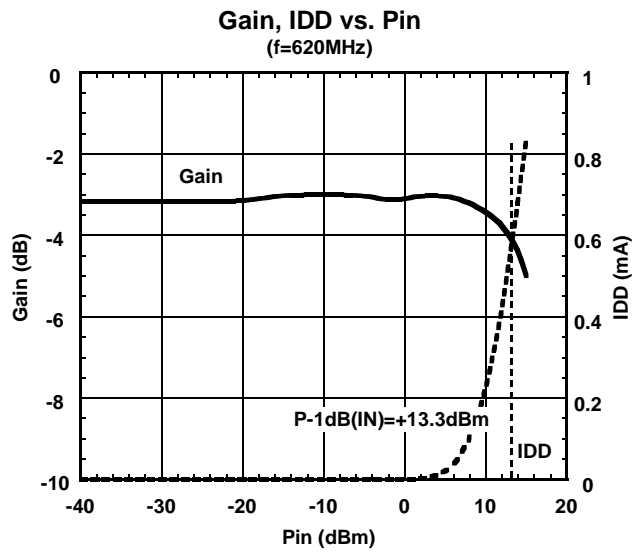
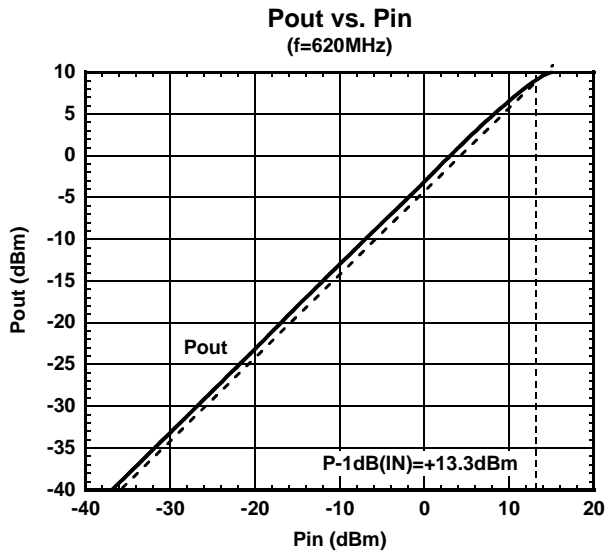
**S<sub>11</sub>, S<sub>22</sub> (50MHz~20GHz)**

**S<sub>21</sub>, S<sub>12</sub> (50MHz~20GHz)**

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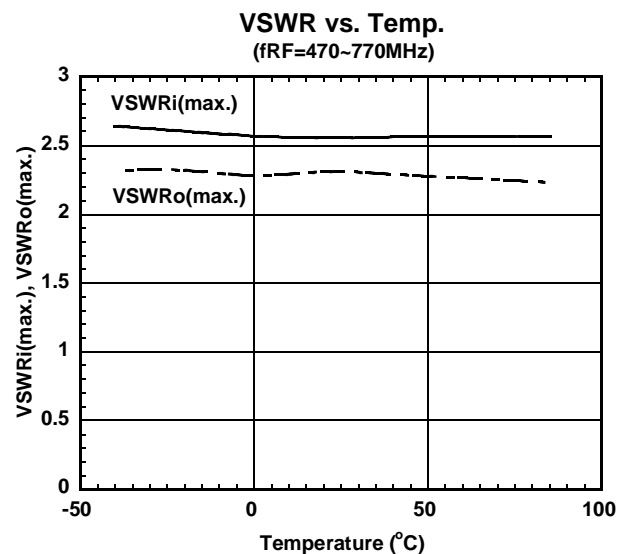
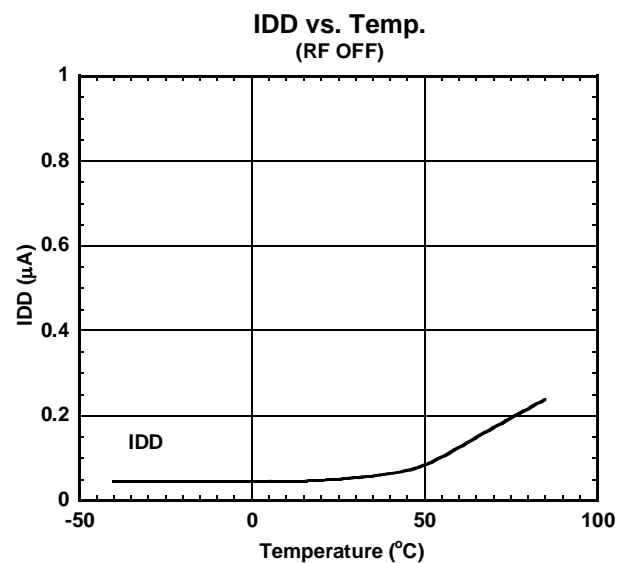
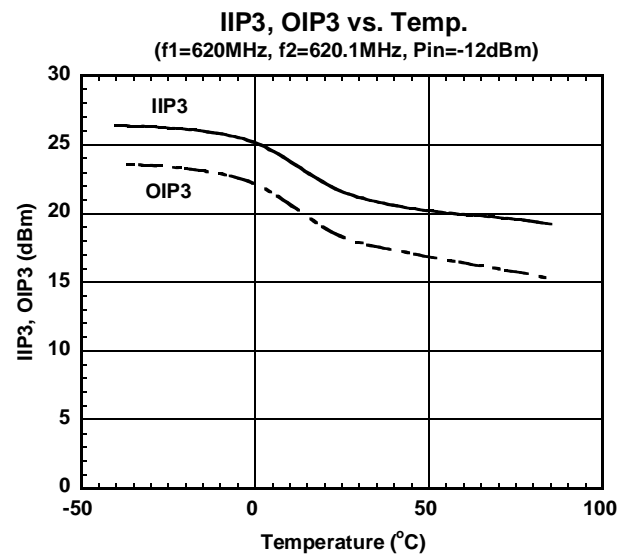
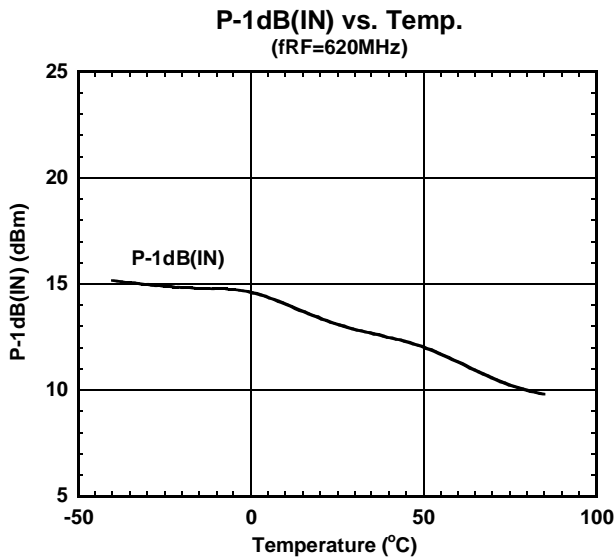
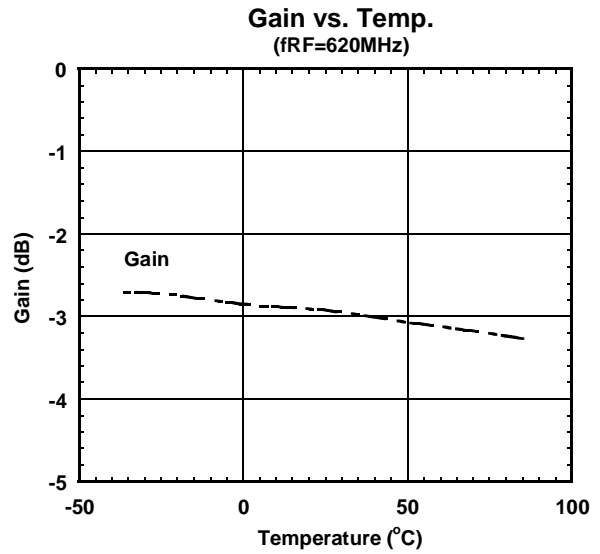
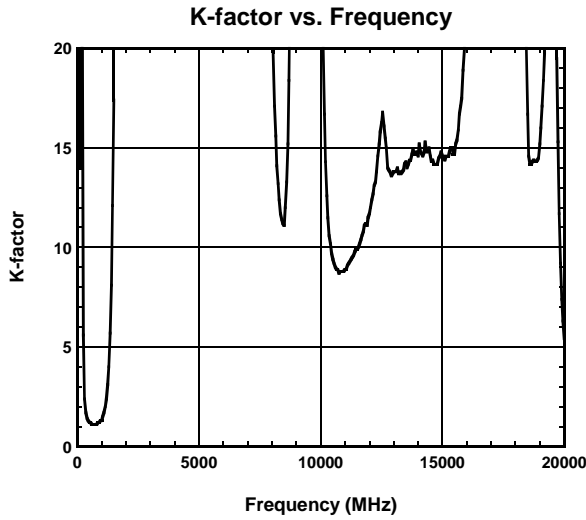
## ■ ELECTRICAL CHARACTERISTICS (Low Gain mode)

Conditions:  $T_a=+25^\circ\text{C}$ ,  $V_{DD}=V_{INV}=2.8\text{V}$ ,  $V_{CTL}=0\text{V}$ ,  $Z_s=Z_l=50\text{ ohm}$ , with application circuit



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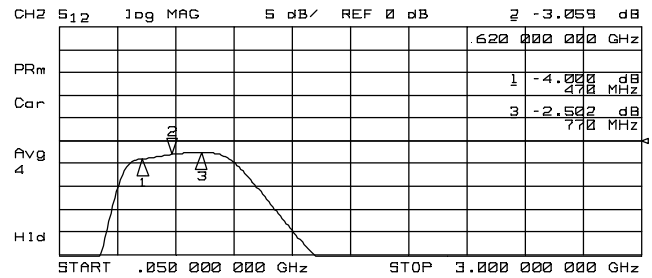
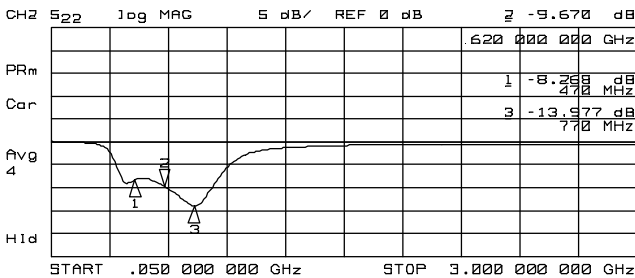
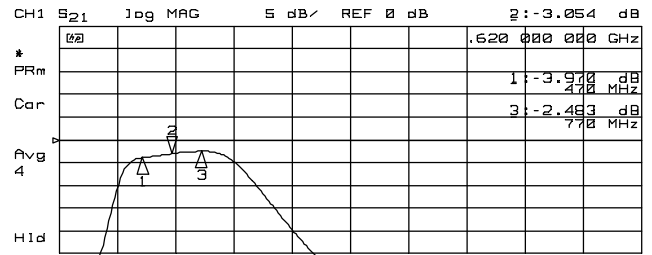
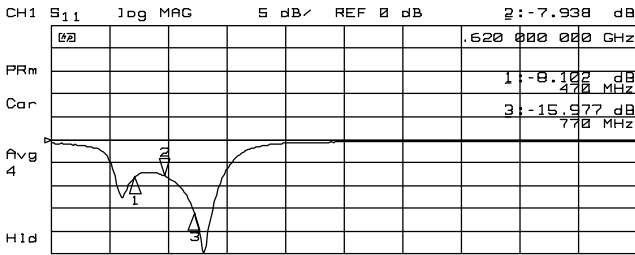
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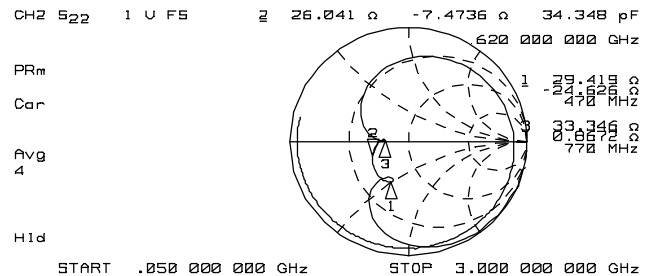
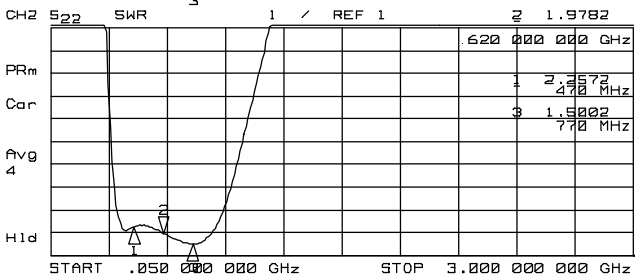
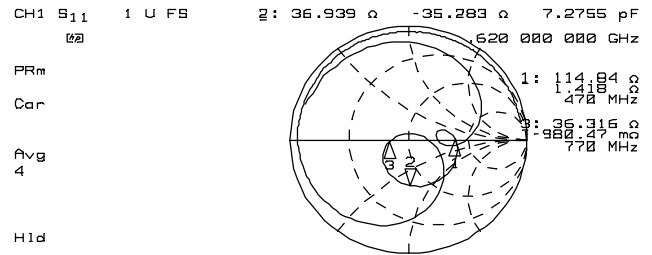
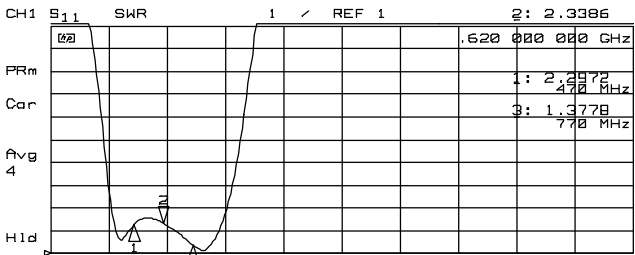
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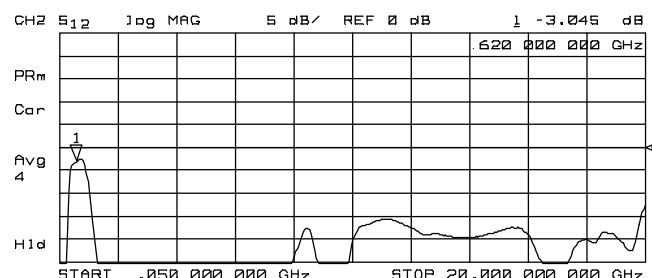
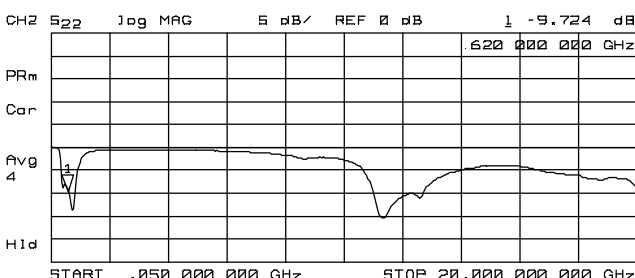
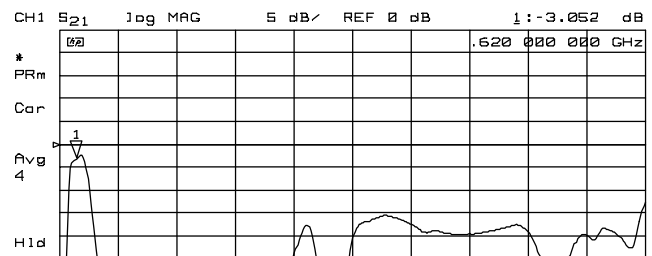
S<sub>11</sub>, S<sub>22</sub>

S<sub>21</sub>, S<sub>12</sub>



VSWR

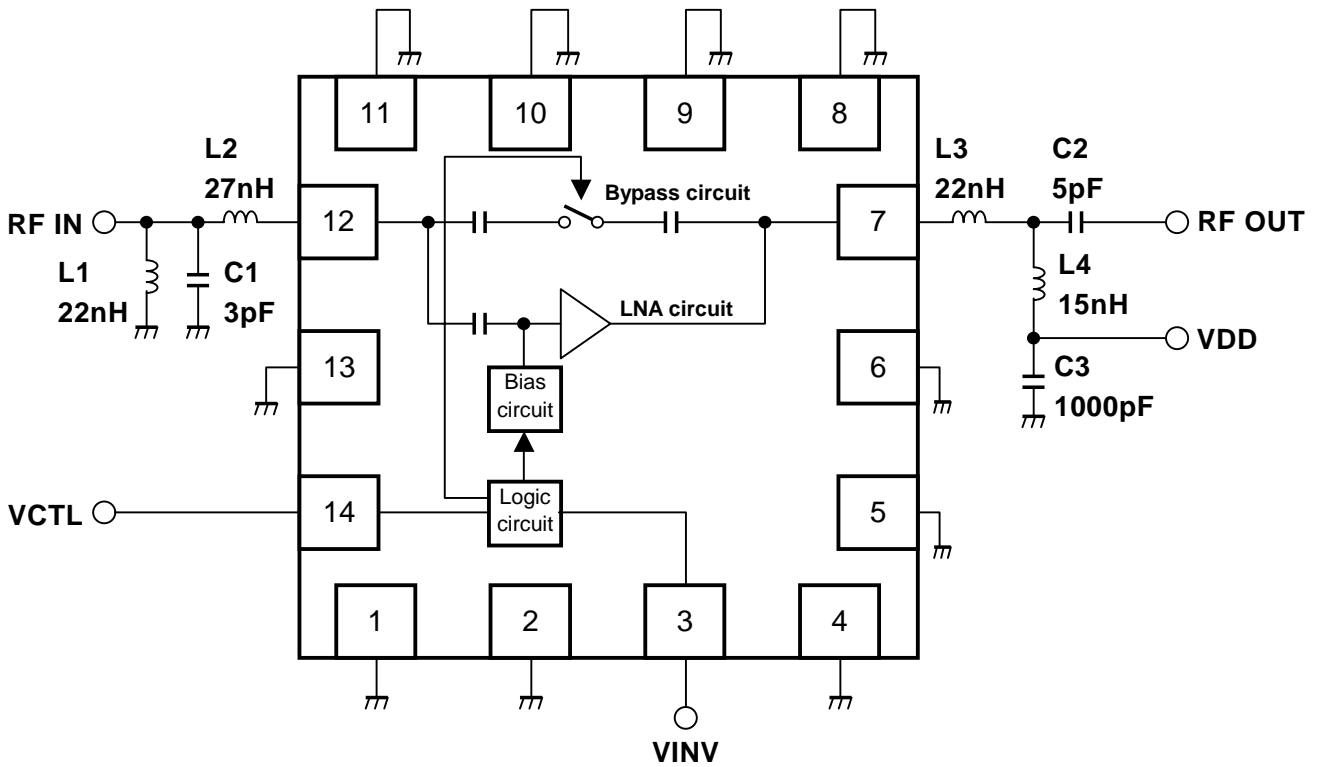
Z<sub>in</sub>, Z<sub>out</sub>



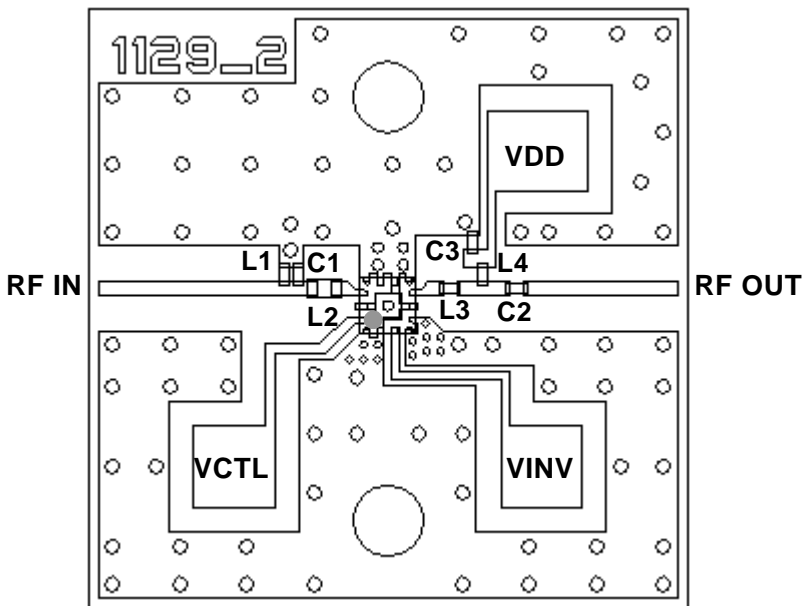
S<sub>11</sub>, S<sub>22</sub> (50MHz~20GHz)

S<sub>21</sub>, S<sub>12</sub> (50MHz~20GHz)

## APPLICATION CIRCUIT



## TEST PCB LAYOUT



### Parts List

Parts ID	Notes
L1, L3, L4	MURATA LQP03T series
L2	TAIYO-YUDEN HK1005 series
C1~C3	MURATA GRM03 series

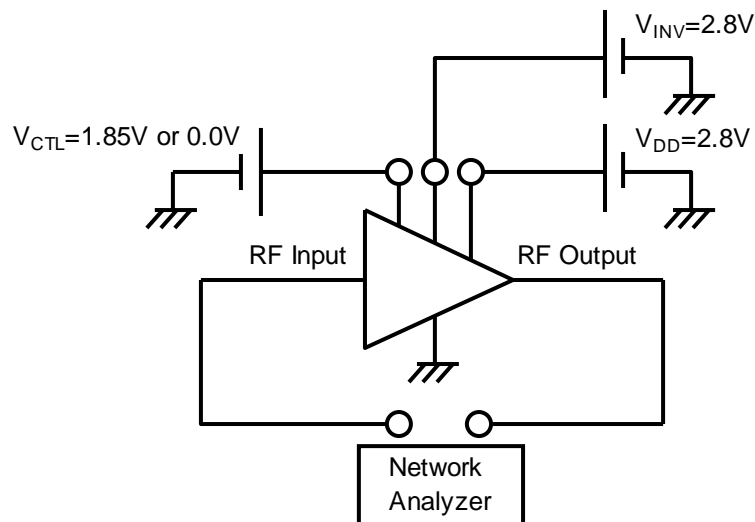
### PCB (FR-4):

t=0.2mm  
 MICROSTRIP LINE  
 WIDTH=0.4mm ( $Z_0=50 \text{ ohm}$ )  
 PCB SIZE=16.8mmx16.8mm

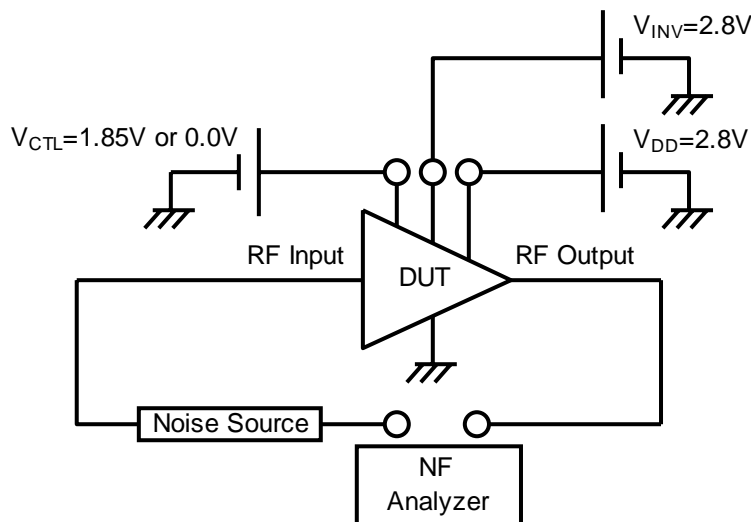
## PRECAUTIONS

- [1] L1-L4, C1 and C2 formed the external matching circuit.
- [2] C3 is a bypass capacitor.
- [3] Ground terminals should be connected with ground plane as close as possible in order to avoid parasitic inductance.
- [4] Please place the ground trace between RFIN(12pin) and RFOUT(7pin) on the top PCB layout to have better isolation between input and output RF ports.
- [5] Please place all external parts around the IC as close as possible.

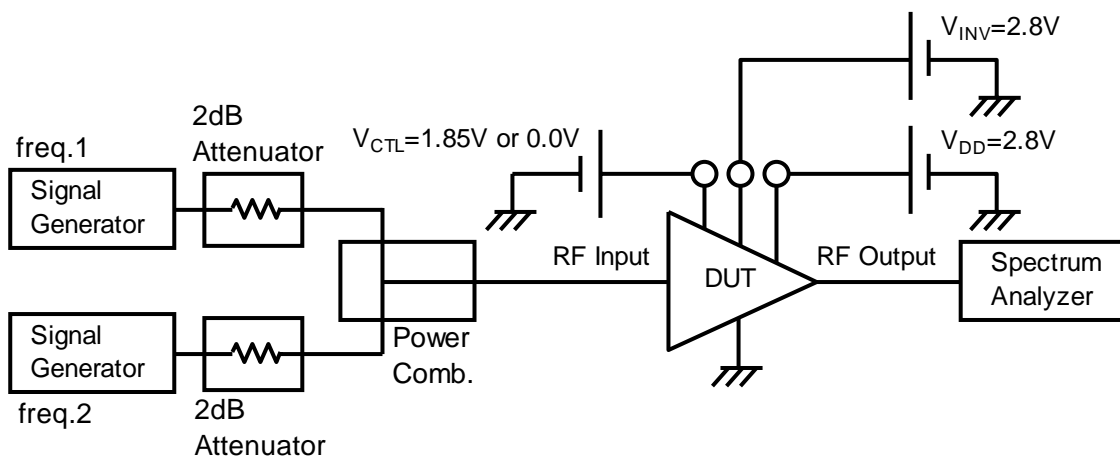
## MEASUREMENT BLOCK DIAGRAM



S parameter Measurement Block Diagram

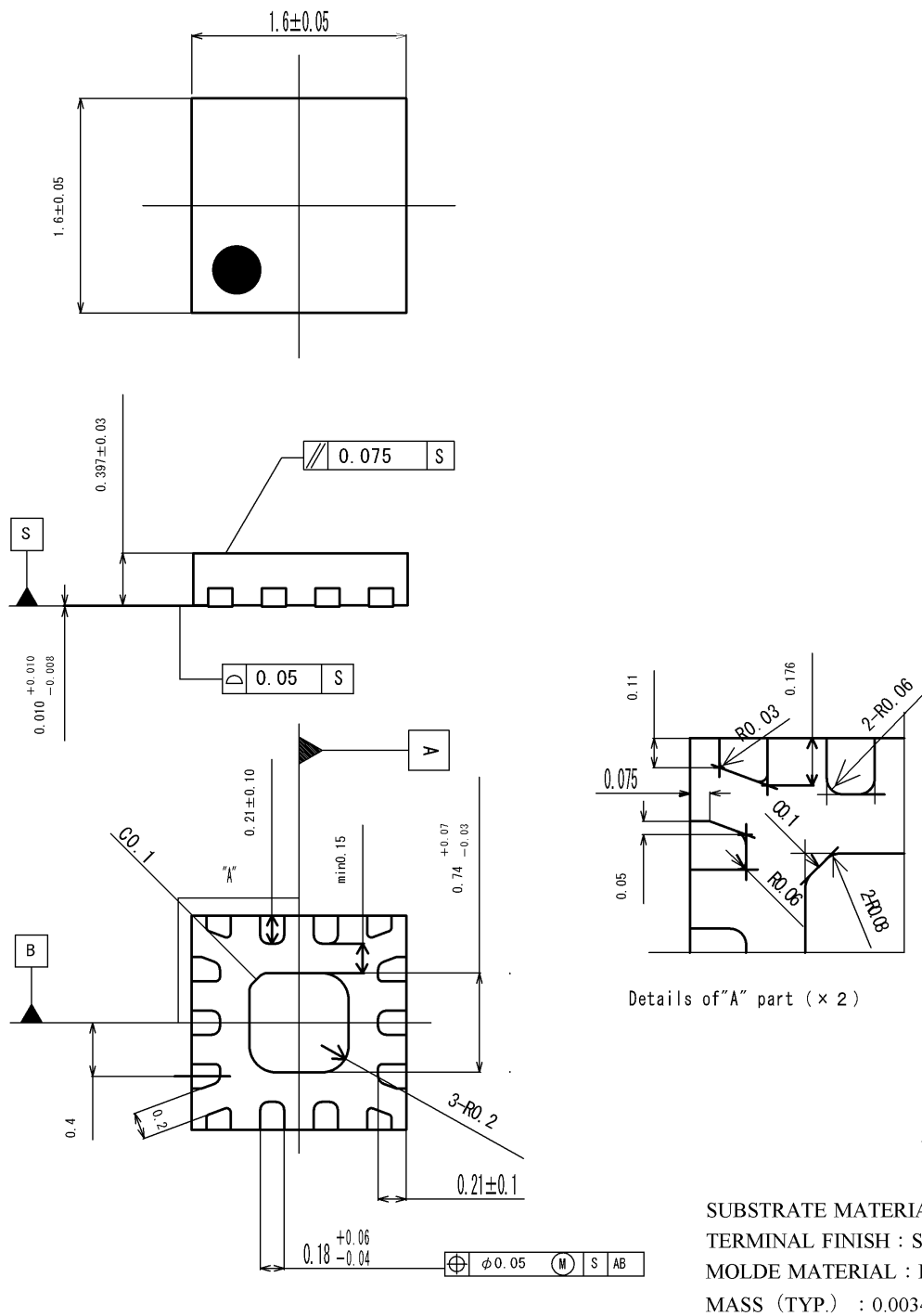


Noise Figure Measurement Block Diagram



Input IP3 Measurement Block Diagram

## ■ PACKAGE OUTLINE (EQFN14-D7)



### Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

### [CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.